

**WHAT IS CLAIMED IS:**

1. A system for automatically generating a hierarchical register consolidation structure, comprising:

a graph generator that parses a High-level Design Language (HDL) file to generate an intermediate graph containing definitions of microprocessor-accessible registers, node interrelationships and summary bits and masks associated with alarm registers;

a graph converter, associated with said graph generator, that selectively adds virtual elements and nodes to said intermediate graph to transform said intermediate graph into a mathematical tree; and

a description generator, associated with said graph converter, that employs said mathematical tree to generate a static tree description in a programming language suitable for use by a device-independent condition management structure.

2. The system as recited in Claim 1 wherein said intermediate graph further contains bit offsets associated with said alarm registers.

3. The system as recited in Claim 1 wherein said description generator further generates an HTML traversable tree representation based on said mathematical tree.

4. The system as recited in Claim 1 wherein said programming  
2 language is C.

5. The system as recited in Claim 1 wherein said HDL file is  
2 produced by a hardware description tool.

6. The system as recited in Claim 1 wherein said condition  
2 management structure interacts only with a logical representation  
3 of said microprocessor-accessible registers, node  
4 interrelationships, summary bits and masks.

7. The system as recited in Claim 1 wherein said graph  
2 generator, said graph converter and said description generator are  
3 embodied in sequences of instructions executable in a general  
4 purpose computing system.

8. A method of automatically generating a hierarchical register consolidation structure, comprising:

parsing a High-level Design Language (HDL) file to generate an intermediate graph containing definitions of microprocessor-accessible registers, node interrelationships and summary bits and masks associated with alarm registers;

selectively adding virtual elements and nodes to said intermediate graph to transform said intermediate graph into a mathematical tree; and

employing said mathematical tree to generate a static tree description in a programming language suitable for use by a device-independent condition management structure.

9. The method as recited in Claim 8 wherein said intermediate graph further contains bit offsets associated with said alarm registers.

10. The method as recited in Claim 8 further comprising employing said static tree description to generate an HTML traversable tree representation based on said mathematical tree.

11. The method as recited in Claim 8 wherein said programming language is C.

12. The method as recited in Claim 8 further comprising  
2 producing said HDL file with a hardware description tool.

13. The method as recited in Claim 8 wherein said condition  
2 management structure interacts only with a logical representation  
3 of said microprocessor-accessible registers, node  
4 interrelationships, summary bits and masks.

14. The method as recited in Claim 8 wherein said parsing,  
2 selectively adding and employing are carried out by sequences of  
3 instructions executable in a general purpose computing system.

15. A system for automatically generating a hierarchical  
2 register consolidation structure, comprising:

3 a graph generator that parses a High-level Design Language  
4 (HDL) file to generate an intermediate graph containing definitions  
5 of microprocessor-accessible registers, node interrelationships and  
6 summary bits, bit offsets and masks associated with alarm  
7 registers;

8 a graph converter, associated with said graph generator, that  
9 selectively adds virtual elements and nodes to said intermediate  
10 graph to transform said intermediate graph into a mathematical  
11 tree; and

12 a description generator, associated with said graph converter,  
13 that employs said mathematical tree to generate a static tree  
14 description in a programming language suitable for use by a device-  
15 independent condition management structure and an HTML traversable  
16 tree representation based on said mathematical tree.

16. The system as recited in Claim 15 wherein said  
2 programming language is C.

17. The system as recited in Claim 15 wherein said HDL file  
2 is produced by a hardware description tool.

18. The system as recited in Claim 15 wherein said condition  
2 management structure interacts only with a logical representation  
3 of said microprocessor-accessible registers, node  
4 interrelationships, summary bits and masks.

19. The system as recited in Claim 15 wherein said graph  
2 generator, said graph converter and said description generator are  
3 embodied in sequences of instructions executable in a general  
4 purpose computing system.

20. The system as recited in Claim 15 wherein said  
2 hierarchical register consolidation structure pertains to a real-  
3 time system.